Amendments to the Claims:

Please cancel claims 1-35, leaving claims 36-45 for examination.

Listing of Claims:

1-35. (Cancelled)

36. (Original) A method of sensing a data state of a memory cell, comprising:

coupling input and output terminals of an integrator circuit according to a first configuration for a first portion of a first time period;

coupling the input and output terminals of the integrator circuit according to a second configuration for a second portion of the first time period; the second configuration changing polarity of the integrator circuit from the first configuration;

based on voltage levels at the output terminals of the integrator circuit, generating a clocked output signal representative of a value; and

averaging the value of the clocked output signal over a second time period.

37. (Original) The method of claim 36, further comprising amplifying the voltage levels at the output terminals of the integrator circuit prior to generating a clocked output signal.

38. (Original) The method of claim 36 wherein the first portion and the second portion of the first time period are equal.

39. (Original) The method of claim 36, further comprising:

providing a first current having a first polarity to a first of the output terminals of the integrator circuit and providing a second current having a second polarity opposite the first polarity to a second of the output terminals of the integrator circuit; and

switching the provision of the first and second currents to the first and second output terminals of the integrator circuit based on the value of the clocked output signal.

40. (Original) The method of claim 36 wherein the second time period is greater than and a multiple of the first time period.

41. (Original) A method of sensing a data state of a memory cell, comprising:

periodically switching coupling of input terminals and output terminals of an integrator circuit from a first configuration to a second configuration, the second configuration changing polarity of the integrator circuit from the first configuration;

periodically comparing output signals provided by the integrator circuit;

based on the comparison, generating an output signal having a voltage representative of a value; and

averaging the value of the output signal over a time period.

42. (Original) The method of claim 41, further comprising amplifying the output signals provided by the integrator signal prior to the periodic comparison.

43. (Original) The method of claim 41, further comprising:

providing a first current having a first polarity to a first of the output terminals of the integrator circuit and providing a second current having a second polarity opposite the first polarity to a second of the output terminals of the integrator circuit; and

switching the provision of the first and second currents to the first and second output terminals of the integrator circuit based on the value of the output signal.

44. (Original) The method of claim 41 wherein the switching occurs at a period greater than at which the comparing occurs.

45. (Original) The method of claim 44 wherein the period of the switching is a multiple of that at which the comparing occurs.